WHAT IS CLAIMED IS:

1. A method of determining a capacitance for use in a circuit simulation, the method comprising:

determining a test structure capacitance of a test structure;

simulating a design structure;

extracting a design structure capacitance of the design structure; and

calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the test structure capacitance from the design structure capacitance.

2. The method of Claim 1, wherein determining the test structure capacitance comprises:

providing a test structure;

simulating the test structure; and

extracting a test structure capacitance of the simulated test structure.

3. The method of Claim 2, wherein the step of extracting the test structure capacitance comprises using three-dimensional capacitance field solving.

4. The method of Claim 1, wherein determining the test structure capacitance comprises physically testing the test structure.

5. The method of Claim 1, wherein determining the test structure capacitance comprises selecting, based on the design structure, a test structure capacitance from a plurality of empirical test structure capacitances, each empirical test structure capacitance being determined by physically testing one of a plurality of different test structures.

6. The method of Claim 1, wherein determining the test structure capacitance comprises selecting, based on the design structure, the test structure capacitance from a plurality of simulated test structure capacitances, each test structure capacitances being extracted from one of a plurality of different test structures using an elaborate capacitance simulator.

7. The method of Claim 1, wherein the step of extracting the design structure capacitance comprises using three-dimensional capacitance field solving.

8. The method of Claim 1, further comprising:

determining an empirical device capacitance by physically testing the test structure; and

calculating a total capacitance of the design structure, wherein calculating the total capacitance comprises adding the parasitic capacitance to the empirical device capacitance.

9. The method of Claim 1, wherein the test structure comprises a gate, a source-drain active area, a contact, and a metal, and wherein the test structure capacitance comprises a gate to source-drain capacitance between the gate and the source-drain active area, a gate to contact capacitance between the gate and the contact, and a gate to metal capacitance between the gate and the metal.

10. The method of Claim 1, further comprising scaling the test structure capacitance based on at least one scaling dimension associated with the design structure.

11. The method of Claim 10, wherein the design structure comprises a gate, and wherein the at least one scaling dimension comprises the width of the gate.

12. The method of Claim 1, wherein the step of providing the test structure comprises selecting the test structure based on one or more geometric boundary conditions associated with the design structure.

13. The method of Claim 12, wherein the design structure comprises a gate and a source-drain active area, and wherein the geometric boundary conditions include the amount of overlap between the gate and the source-drain active area.

14. The method of Claim 12, wherein the design structure comprises a gate oxide layer, and wherein the geometric boundary conditions include the thickness of the gate oxide layer.

15. The method of Claim 12, wherein the design structure comprises a body and a source-drain active area, and wherein the geometric boundary conditions include the spacing between the body and the source-drain active area.

16. The method of Claim 1, further comprising:

providing a calibration structure having one or more boundary conditions;

determining a target calibration structure capacitance of the calibration structure;

simulating the calibration structure;

extracting a test calibration structure capacitance of the simulated calibration structure using a first simulator;

calculating the difference between the test calibration structure capacitance and the target calibration structure capacitance;

determining if the difference is satisfactory according to an accuracy criterion; and

adjusting at least one of the one or more boundary conditions if the difference is unsatisfactory according to the accuracy criterion; and

wherein determining the test structure capacitance comprises determining the test structure capacitance of a test structure having boundary conditions which match the boundary conditions of the calibration structure, including any adjusted boundary conditions.

17. The method of Claim 16, wherein the step of determining the test structure capacitance comprises:

providing a test structure having boundary conditions which match the boundary conditions of the calibration structure, including any adjusted boundary conditions;

simulating the test structure; and

extracting a test structure capacitance of the simulated test structure;

wherein the test structure capacitance and the design structure capacitance are extracted using the first simulator.

18. The method of Claim 16, wherein the target calibration structure capacitance is determined by physically testing the calibration structure.

19. The method of Claim 16, wherein the target calibration structure capacitance is determined by:

simulating the calibration structure; and

extracting a calibration structure capacitance of the simulated calibration structure using a second simulator.

20. The method of Claim 19, wherein the second simulator is an elaborate capacitance simulator.

21. A method of determining a capacitance for use in a circuit simulation, the method comprising:

selecting a test structure based on one or more geometric boundary conditions associated with a design structure, the test structure comprising a gate, a source-drain active area, a contact, and a metal;

simulating the test structure;

extracting a test structure capacitance of the simulated test structure, the test structure capacitance comprising a gate to source-drain capacitance between the gate and the source-drain active area, a gate to contact capacitance between the gate and the contact, and a gate to metal capacitance between the gate and the metal;

simulating the design structure;

extracting a design structure capacitance of the simulated design structure; and

scaling the test structure capacitance based on at least one scaling dimension associated with the design structure; and

calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the test structure capacitance from the design structure capacitance.

22. The method of Claim 21, wherein the at least one scaling dimension comprises the width of the gate.

23. The method of Claim 21, wherein the geometric boundary conditions include the amount of overlap between the gate and the source-drain active area.

24. The method of Claim 21, wherein the design structure comprises a gate oxide layer, and wherein the geometric boundary conditions include the thickness of the gate oxide layer.

25. The method of Claim 21, wherein the design structure comprises a body, and wherein the geometric boundary conditions include the spacing between the body and the source-drain active area.

26. A method of determining a capacitance for use in a circuit simulation, the method comprising:

selecting a design structure at least partially defined by one or more design structure parameters;

determining a design structure capacitance of the design structure;

determining a desired test structure capacitance based on the one or more design structure parameters and the test structure data, a set of test structure data including information regarding a plurality of test structures, the information including a test structure capacitance and one or more test structure parameters associated with each of the plurality of test structures; and

calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the desired test structure capacitance from the design structure capacitance.

27. The method of Claim 26, wherein:

the design structure comprises a design structure gate and a design structure contact, and the one or more design structure parameters comprises a distance between the design structure gate and the design structure contact; and

each of the plurality of test structures comprises a test structure gate and a test structure contact, and the one or more test structure parameters associated with each of the plurality of test structures comprises a distance between the test structure gate and the test structure contact.

28. The method of Claim 26, wherein:

the design structure comprises a design structure first contact and a design structure second contact, and the one or more design structure parameters comprises a distance between the design structure first contact and the design structure second contact; and

each of the plurality of test structures comprises a test structure first contact and a test structure second contact, and the one or more test structure parameters associated with each of the plurality of test structures comprises a distance between the test structure first contact and the test structure second contact.

29. The method of Claim 26, wherein the test structure capacitance associated with each of the plurality of test structures is determined by:

simulating each test structure;

extracting a test structure capacitance of each simulated test structure; and

scaling each test structure capacitance based on at least one scaling dimension associated with the design structure.

30. The method of Claim 29, wherein the step of extracting each test structure capacitance comprises using three-dimensional capacitance field solving.

31. The method of Claim 29, the test structure data further including an empirical device capacitance associated with each of the plurality of test structures determined by physically testing each of the test structures, wherein the method further includes:

determining a desired empirical device capacitance based on the one or more design structure parameters and the test structure data; and

calculating a total capacitance of the design structure, wherein calculating the total capacitance comprises adding the parasitic capacitance to the select empirical device capacitance.

32. The method of Claim 26, wherein the test structure capacitance associated with each of the plurality of test structures is determined by physically testing each test structure.

33. The method of Claim 26, wherein the design structure capacitance is determined by:

simulating the design structure; and

extracting a design structure capacitance of the simulated design structure.

34. The method of Claim 33, wherein the step of extracting the design structure capacitance comprises using three-dimensional capacitance field solving.

35. The method of Claim 26, wherein at least one of the one or more design structure parameters is different from at least one of the one or more test structure parameters associated with each of the plurality of test structures, and wherein determining the desired test structure capacitance comprises using an algorithm to a desired test structure capacitance.

36. An apparatus for simulating the operation of a circuit, the apparatus comprising a computer system which includes a processor and a memory that stores computer program code executable by the processor, the computer program code comprising a circuit simulator program which receives input regarding a component of the circuit, the input comprising a device model and a parasitic capacitance of a design structure of the component, the parasitic capacitance being determined using a test structure capacitance associated with a test structure and a design structure capacitance associated with the design structure, wherein the processor is operable to execute the circuit simulator program to output performance characteristics of the circuit based at least in part on the parasitic capacitance and the device model of the design structure.

37. The apparatus of Claim 36, wherein the parasitic capacitance received as input by the simulator program is determined by deducting the test structure capacitance from the design structure capacitance

38. The method of Claim 36, wherein the test structure capacitance is determined by:

simulating the test structure; and

extracting a test structure capacitance of the simulated test structure.

39. The method of Claim 38, wherein the test structure capacitance is determined by physically testing the test structure.

40. The method of Claim 36, wherein the design structure capacitance is determined by:

simulating the design structure; and

extracting a design structure capacitance of the simulated design structure.

41. The apparatus of Claim 36, wherein the device model received as input by the simulator program includes an empirical device capacitance of the test structure obtained by physically testing the test structure.

42. The apparatus of Claim 36, wherein the device model received as input by the simulator program includes a device capacitance of the test structure, and wherein the device capacitance is effectively set at zero.

43. The apparatus of Claim 36, wherein the test structure used to calculate the parasitic capacitance is selected based on one or more geometric boundary conditions associated with the design structure.

44. The apparatus of Claim 36, wherein the memory further stores parasitic capacitance data accessible by the processor, the parasitic capacitance data comprising a plurality of parasitic capacitances each corresponding to one of a plurality of structures, wherein the parasitic capacitance received as input into the simulator program is selected from the plurality of parasitic capacitances based on one or more parameters of the design structure.

45. The apparatus of Claim 44, wherein the design structure comprises a gate and a contact, and wherein the parameters of the design structure include the spacing between the first contact and the gate.

46. The apparatus of Claim 44, wherein the design structure comprises a first contact and a second contact, and wherein the parameters of the design structure include the spacing between the first contact and the second contact.

47. An electronic apparatus, at least a portion of the electronic apparatus designed using a circuit simulation, the circuit simulation receiving a parasitic capacitance of a design structure, the parasitic capacitance determined by:

providing a test structure;

simulating the test structure;

extracting a test structure capacitance of the simulated test structure;

simulating a design structure;

extracting a design structure capacitance of the simulated design structure; and

calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the test structure capacitance from the design structure capacitance.

48. The electronic apparatus of Claim 47, wherein the circuit simulation further receives a device model of a design structure, the device model including an empirical design structure capacitance of the design structure obtained by physically testing the design structure.

49. The electronic apparatus of Claim 47, further comprising selecting the test structure based on one or more geometric boundary conditions associated with the design structure.